Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

What is claimed is:

Claim 1 (Currently Amended) A pipelined fast Fourier transform (FFT) processor for receiving an input sequence, the processor comprising:

at least one FFT triplet module having first, second and third butterfly modules connected in series by selectable multipliers for selectively performing trivial ~~co-efficient~~ coefficient multiplication and complex ~~co-efficient~~ coefficient multiplication on output data sequences of adjacent butterfly modules, the selection being responsive to a step-counter provided with each butterfly module, each of the at least one FFT triplet modules terminating in a twiddle factor multiplier for applying a twiddle factor to an output of the third butterfly module of the respective triplet module, the at least one FFT triplet module for receiving ~~the~~ an input data sequence and for outputting a final output data sequence representing an FFT of the input data sequence.

Claim 2 (Original) The processor of claim 1, wherein each butterfly module includes a radix-2 butterfly unit and a feedback memory.

Claim 3 (Original) The processor of claim 2, wherein, for an input sequence of N samples, an output sequence $X(k,n)$ of each butterfly module is equal to $x(n)+(-1)^k x\left(n+\frac{N}{2}\right)$.

Claim 4 (Currently Amended) The processor of claim 1, wherein at least one of the selectable multipliers for performing trivial ~~co-efficient~~ coefficient multiplication is integrated in an adjacent butterfly module.

Claim 5 (Original) The processor of claim 1, wherein the selectable multipliers each include a multiplier and a switch for bypassing the multiplier.

Claim 6 (Currently Amended) The processor of claim 1, wherein the first and second butterfly modules are connected by a selectable multiplier for selectively applying trivial ~~co-~~

~~efficient~~ coefficient multiplication.

Claim 7 (Currently Amended) The processor of claim 7, wherein the second and third butterfly modules are connected by a selectable multiplier for performing trivial ~~co-efficient~~ coefficient multiplication and a selectable multiplier for performing the complex ~~co-efficient~~ coefficient multiplication $W_N^{N/8}$.

Claim 8 (Original) The processor of claim 2, wherein, for an input sequence having *N* samples, the feedback memories for the first, second and third butterfly modules hold *N*/2, *N*/4 and *N*/8 samples, respectively.

Claim 9 (Original) The processor of claim 1 wherein the input sequence is of length *N*, where $(\log_2 N) \bmod 3 = 1$, the processor having a plurality of FFT triplets in seriatim and further including an FFT terminator having a butterfly unit and a corresponding memory sized to hold a single sample, the FFT terminator for receiving the output sequence from the final twiddle factor multiplier and for performing a butterfly operation on the received output sequence to render an FFT of the input sequence.

Claim 10 (Original) The processor of claim 1 wherein the input sequence is of length *N*, where $(\log_2 N) \bmod 3 = 2$, the processor having a plurality of FFT triplets in seriatim and further including an FFT terminator having first and second butterfly units having corresponding memories sized to hold two samples and a single sample respectively, the first butterfly unit connected to the second butterfly unit by a selectable multiplier for selectively multiplying the output of the first butterfly unit by *–j*, the FFT terminator for receiving the output sequence from the final twiddle factor multiplier and for performing a pair of butterfly operations on the received output sequence to render an FFT of the input sequence.

Claim 11 (Original) The processor of claim 1, wherein the twiddle factor multiplier is a cordic rotator.

Claim 12 (Currently Amended) A pipelined fast Fourier transform (FFT) processor for receiving an input data sequence of *N* samples, the processor comprising:

at least one FFT triplet module, the triplet module having:

a first FFT stage module having a first stage radix-2 butterfly unit for receiving the input data sequence and for providing a first stage output sequence in accordance with a butterfly

operation performed on the input data sequence, the first stage radix-2 butterfly unit having a first feedback memory connected thereto;

a second FFT stage module having a selectable multiplier for selectively multiplying the first stage output sequence by a trivial ~~co-efficient~~ coefficient, the selection being responsive to a step-counter provided with the second FFT stage module, and a second stage radix-2 butterfly unit for providing a second stage output sequence in accordance with the butterfly operation performed on the output of the selectable multiplier, the second stage radix-2 butterfly unit having a second feedback memory connected thereto; and

a third FFT stage module having a multiply selectable multiplier for selectively multiplying the second stage output sequence by at least one of the trivial ~~co-efficient~~ coefficient and a complex ~~co-efficient~~ coefficient, the selection being responsive to a step-counter provided with the third FFT stage module, a third stage radix-2 butterfly unit for providing a butterfly output in accordance with the butterfly operation performed on the output of the multiply selectable multiplier, the third stage radix-2 butterfly unit having a third feedback memory connected thereto, and a multiplier for multiplying the butterfly output by a twiddle factor, to provide an output data sequence corresponding to an FFT of the input data sequence.

Claim 13 (Original) The FFT processor of claim 12, wherein each of the first, second and third stage output sequences $X(k,n)$ is equal to $x(n)+(-1)^k x\left(n+\frac{N}{2}\right)$.

Claim 14 (Currently Amended) The FFT processor of claim 12, wherein at least one of the butterfly units includes an integrated pre-multiplication function for applying a trivial ~~co-efficient~~ coefficient multiplication to a received input sequence.

(Deleted - Previously Unnumbered) ~~The FFT processor of claim 12, further including an FFT terminator determined in accordance with the length *N* of the input sequence.~~

Claim 15 (Currently Amended) A pipelined fast Fourier transform (FFT) processor for receiving an input data sequence of *N* samples, the processor comprising:

at least one FFT triplet module, the triplet module having:

a first FFT stage module having a first stage radix-2 butterfly unit for receiving the input data sequence and for providing a first stage output sequence in accordance with a butterfly operation performed on the input data sequence, the first stage radix-2 butterfly unit having a first feedback memory connected thereto;

a second FFT stage module having a multiply selectable multiplier for selectively multiplying the first stage output sequence by at least one of the trivial ~~co-efficient~~ coefficient and a constant complex ~~co-efficient~~ coefficient, the selection being responsive to a step-counter provided with the second FFT stage module, and a second stage radix-2 butterfly unit for providing a second stage output sequence in accordance with the butterfly operation performed on the output of the selectable multiplier, the second stage radix-2 butterfly unit having a second feedback memory connected thereto; and

a third FFT stage module having a selectable multiplier for selectively multiplying the second stage output sequence by a trivial ~~co-efficient~~ coefficient, the selection being responsive to a step-counter provided with the third FFT stage module, a third stage radix-2 butterfly unit for providing a butterfly output in accordance with the butterfly operation performed on the output of the selectable multiplier, the third stage radix-2 butterfly unit having a third feedback memory connected thereto, and a multiplier for multiplying the butterfly output by a twiddle factor, to provide an output data sequence corresponding to an FFT of the input data sequence.

Claim 16 (Original) The FFT processor of claim 15, wherein each of the first, second and third stage output sequences $X(k,n)$ is equal to $x(n)+(-1)^k x(n+\frac{N}{2})$.

Claim 17 (Currently Amended) The FFT processor of claim 15, wherein at least one of the butterfly units includes an integrated pre-multiplication function for applying a trivial ~~co-efficient~~ coefficient multiplication to a received input sequence.

Claim 18 (Original) The FFT processor of claim 15, further including an FFT terminator determined in accordance with the length *N* of the input sequence.

Claim 19 (Original) The FFT processor of claim 18, wherein the FFT terminator includes a butterfly module having a memory sized to store a single sample, for receiving as a terminator input, the output of the third FFT stage multiplier and for performing a butterfly operation on the terminator input to render an FFT of the input sequence of *N* samples.

Claim 20 (Original) The FFT processor of claim 18, wherein the FFT terminator includes a first butterfly module having a memory sized to store a pair of samples, for receiving as a terminator input, the output of the third stage multiplier and for performing a butterfly operation on the terminator input, and a second butterfly module connected to the

first butterfly module of the terminator by a selectable multiplier, the selectable multiplier for selectively multiplying the output of the first butterfly module of the terminator by *–j*, the second butterfly module having a memory sized to store a single sample and for performing a butterfly operation on the selectively multiplied output of the first butterfly module of the terminator to render an FFT of the output sequence.

Claim 21 (Currently Amended) A method of performing an FFT on a data sequence of *N* samples in an FFT processor having a butterfly module, the method comprising:

for all integers x according to $1 \le x \le \log_2 N$, repeating the steps of

receiving and buffering $\frac{N}{2^x}$ samples at a time from a sequence having *N* samples;

generating a 2-point FFT using the n^{th} and the $\left(n+\frac{N}{2^x}\right)^{th}$ samples;

responsive to a step-counter provided with the butterfly module, selectively multiplying the generated 2-point FFT sequence by a complex valued multiplicand; and

terminating the FFT using a termination sequence determined in accordance with a $(\log_2 N) \bmod 3$ relationship.

Claim 22 (Currently Amended) The method of claim 21 wherein the complex valued multiplicand is selected from a list including 1, *-j*, $\frac{\sqrt{2}}{2} - j\frac{\sqrt{2}}{2}$, and a complex twiddle factor ~~co-efficient~~ coefficient.

Claim 23 (Original) The method of claim 21 wherein $(\log_2 N) \bmod 3 = 1$ and the step of terminating the FFT includes buffering a sample received from the final selective multiplication and performing a 2-point FFT using the buffered sample and the subsequent sample in the sequence to obtain the FFT of the sequence of *N* samples.

Claim 24 (Original) The method of claim 21 wherein $(\log_2 N) \bmod 3 = 2$ and the step of terminating the FFT includes:

buffering a pair of samples received from the final selective multiplication and performing pair-wise 2-point FFTs using the two buffered samples and the two subsequent samples in the sequence;

selectively multiplying the result of the pair-wise 2 point FFT by $-j$; and

buffering a sample received from the selective multiplication of the pair-wise 2-point FFT and performing a 2-point FFT using the buffered sample and the subsequent sample in the sequence to obtain the FFT of the sequence of N samples.

Claim 25 (New) The FFT processor of claim 12, further including an FFT terminator determined in accordance with the length N of the input sequence.